Dkt: 884.826US1 (INTEL)

Title: HYBRID PACKAGE WITH NON-INSERTABLE AND INSERTABLE CONDUCTIVE FEATURES, COMPLEMENTARY RECEPTACLE, AND METHODS OF FABRICATION, ASSEMBLY, AND OPERATION THEREFOR

Assignee: Intel Corporation

IN THE CLAIMS

Please amend the claims as follows:

- 1. (Previously Presented) An electronic circuit package comprising:

 at least one non-insertable feature at a first surface of the electronic circuit package; and
 at least one conductive, low insertion force, insertable feature extending perpendicularly
 from the first surface in a vertical direction, wherein the at least one conductive, low insertion
 force, insertable feature contacts conductive structures within the electronic circuit package, and
 wherein the at least one conductive, low insertion force, insertable feature is configured to
 receive a horizontal force, provided by a horizontal force mechanism, to engage the at least one
 conductive, low insertion force, insertable feature with a receptacle.
- 2. (Original) The electronic circuit package as claimed in claim 1, wherein the electronic circuit package comprises an integrated circuit package.
- 3. (Original) The electronic circuit package as claimed in claim 1, wherein the at least one non-insertable feature includes a land grid array land.
- 4-5. (Canceled)
- 6. (Original) The electronic circuit package as claimed in claim 1, wherein a total feature count is greater than 400 features, and the total feature count is a sum of a first number of non-insertable features and a second number of insertable features.
- 7. (Original) The electronic circuit package as claimed in claim 1, wherein the at least one non-insertable feature is coupled to circuits that use or produce input/output signals, and the at least one insertable feature is electrically coupled to circuits that consume power or require ground connection.

Dkt: 884.826US1 (INTEL) Serial Number: 10/608,050

Title: HYBRID PACKAGE WITH NON-INSERTABLE AND INSERTABLE CONDUCTIVE FEATURES, COMPLEMENTARY RECEPTACLE, AND METHODS OF FABRICATION, ASSEMBLY, AND OPERATION THEREFOR

Assignee: Intel Corporation

8-34. (Canceled)

(Previously Presented) A receptacle comprising: 35.

a body;

at least one non-insertable, land grid array contact having contact portions exposed at a first surface of the body of the receptacle;

at least one insertable contact having an opening on the first surface and conductive structures within the body of the receptacle, wherein the at least one non-insertable contact and the at least one insertable contact are arranged to make electrical contact with non-insertable features and insertable features of a single electronic circuit package brought into contact with the receptacle; and

electrical interfaces on a second surface of the body of the receptacle, wherein the electrical interfaces are electrically connected to the at least one non-insertable, land grid array contact and the at least one insertable contact.

- (Previously Presented) The receptacle as claimed in claim 35, wherein the receptacle 36. comprises a socket.
- (Previously Presented) The receptacle as claimed in claim 35, wherein the receptacle 37. comprises an interposer.